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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/868,322	06/18/2001	Yojiro Matsueda	109503	9116
25944	7590	03/31/2004	EXAMINER	
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			NGUYEN, JENNIFER T	
			ART UNIT	PAPER NUMBER
			2674	10

DATE MAILED: 03/31/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/868,322	MATSUEDA, YOJIRO	
	Examiner	Art Unit	
	Jennifer T Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 18 June 2001.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-26 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-26 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____.
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____.

DETAILED ACTION

1. This Office action is responsive to amendment filed on 03/23/2004.
2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 2, 5, 6, 9-23, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al. (U.S. Patent No. 5,815,136) in view of Motegi et al. (U.S. Patent No. 6,025,822).

Regarding claims 1 and 2, referring to Figs. 47A and 47B, Ikeda teaches a display device, comprising: a display drive (2451) having a plurality of scanning lines and a plurality of data lines formed in a grating form corresponding to dots as minimum units of display and active elements provided corresponding to intersections, the display drive (2451) performs display control using a liquid crystal by driving the scanning lines and the data lines; a scanning line driver (2449) that selects and drives the scanning lines, the scanning line driver being allocated corresponding to a length in a column direction of the display drive (2451); a memory (2425) having a plurality of memory cells that are capable of storing an image signal for performing display control of dots in at least one row of the display drive (2451), the memory being allocated corresponding to the length in a row direction of the display drive (2451); a column

decoder (2443) allocated corresponding to the length in the row direction of the display drive (2451), the column decoder (2443) selects the memory cells for storing an input-image signal; a column selection switch section (2445) allocated corresponding to the length in the row direction of the display drive (2451), to switch on the basis of a selection by the column decoder (2443) and the image signal and storing the image signal to said memory cells selected by said column decoder (2443); and a data line driver (2405) allocated corresponding to, the length in the row direction of the display drive, the data line driver drives (2405) said data lines on the basis of the image signal stored in the memory (2425), the data line driver (2405) further being integrated on a semiconductor or an insulating substrate and integrally formed therewith (from col. 31, line 40 to col. 33, line 67 and col. 34, lines 28-65).

Ikeda differs from claims 1 and 2 in that he does not specifically teach display drive and memory cells further being integrated on a semiconductor. However, referring to Fig. 1, Motegi teaches display drive (101) and memory cells (10) being integrated on a semiconductor (see abstract, from col. 9, line 26 to col. 11, line 10). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the display drive and memory cells further being integrated on a semiconductor as taught by Motegi in the system of Ikeda in order to provide a driving circuit can be small-sized as a whole, according power consumption in the driving circuit can be reduced. As a result, the application of the driving circuit to a small terminal device can be easy.

Regarding claims 5 and 6, referring to Figs. 47A and 47B, Ikeda teaches a display device, comprising: a display drive (2451) having a plurality of scanning lines and a plurality of bit lines, and a liquid crystal display that is controlled by driving the corresponding scanning lines and bit

lines and provided on a dot-by-dot basis as minimum units of display control, and formed in a matrix form; a memory (2425) having a plurality of memory cells that are capable of storing an image signal for performing display control of dots in at least one row of the display drive, the memory (2425) being allocated corresponding to the length in the row direction of the display drive (2451); a column decoder (2443) allocated corresponding to the length in the row direction of the display drive (2451), the column decoder (2443) selects the memory cells for storing an input image signal; and a column selection switch (2445) section allocated corresponding to the length in the row direction of the display drive (2451), to switch on the basis of a selection by the column decoder (2443) and the image signal and storing the image signal to said memory cell selected by the column decoder (2443), the column decoder (2443) being integrated on a semiconductor or insulating substrate and integrally formed therewith (from col. 31, line 40 to col. 33, line 67 and col. 34, lines 28-65).

Ikeda differs from claims 5 and 6 in that he does not specifically teach display drive and memory cells further being integrated on a semiconductor. However, referring to Fig. 1, Motegi teaches display drive (101) and memory cells (10) being integrated on a semiconductor (see abstract, from col. 9, line 26 to col. 11, line 10). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the display drive and memory cells further being integrated on a semiconductor as taught by Motegi in the system of Ikeda in order to provide a driving circuit can be small-sized as a whole, according power consumption in the driving circuit can be reduced. As a result, the application of the driving circuit to a small terminal device can be easy.

Regarding claims 9 and 10, Ikeda further teaches the number of the memory cells, which are allocated corresponding to the length in the row direction of said display drive and capable of storing the image signal for display control of the dots on one row of said display drive, is structured redundantly (col. 33, lines 27-67).

Regarding claims 11 and 12, Ikeda further teaches on the basis of an address signal representative of a display position and a storage position, said scanning line driver selects the scanning lines and the word line driver selects said word lines (Fig. 1A, col. 9, lines 19-67).

Regarding claim 13, Ikeda further teaches independent address signals are inputted to the scanning line driver and the word line driver (Fig. 1A, col. 9, lines 19-67).

Regarding claim 14, Ikeda further teaches the scanning line driver operates to select and drive the scanning lines on the basis of the address signal only when a scanning line driver control signal is inputted, and the word line driver operates to select and drive the word lines on the basis of the address signal only when a word line driver control signal is inputted (Fig. 1A, col. 9, lines 19-67).

Regarding claim 15, Ikeda further teaches the column decoder section (2443) selecting the memory cell to store an inputted image signal on the basis of the address signal (from col. 31, line 42 to col. 32, line 58).

Regarding claims 16 and 17, the combination of Ikeda and Motegi teaches one pixel comprises three dots of developing and display red, blue, and green as light source colors (col. 3, lines 11-55 of Motegi), the image signal is inputted on the basis of a unit of one-pixel, and said column decoder selects the memory cell in an amount of one pixel (from col. 17, line 22 to col. 18, line 65 of Ikeda).

Regarding claim 18, further Ikeda teaches an input interconnection for the image signal to be stored in the memory cell (2425) and the column selection switch section (2445) are formed on a side opposite to the display drive (2451) sandwiching said memory there between (from col. 31, line 40 to col. 32, line 58).

Regarding claims 19-22, Ikeda further teaches the memory (2425) is allocated with the memory cell corresponding to the length in the row direction of said display drive (2451) and formed in a multi-stage structure (from col. 31, line 40 to col. 33, line 67 and col. 34, lines 28-65).

Regarding claim 23, Ikeda further teaches a timing controller (2409) that controls a timing of transmitting the address signal, and a memory controller (2418) that controls the transmitting of the image signal, the memory controller (2418) being integrated on a semiconductor or an insulating substrate and integrally formed therewith (from col. 31, line 40 to col. 32, line 58).

Regarding claim 25, Ikeda further teaches the display drive (2451) and the memory (2425) are directly coupled to supply the image signal comprising a digital signal stored in the memory (2425) to said display drive (2451) (from col. 31, line 40 to col. 32, line 58).

Regarding claim 26, Ikeda further teaches the display drive performs digital drive through area tonal level (from col. 31, line 40 to col. 32, line 58).

5. Claims 3, 4, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al. (U.S. Patent No. 5,815,136) in view of Motegi et al. (U.S. Patent No. 6,025,822).

Regarding claims 3, 4, 7, and 8, the combination of Ikeda and Motegi teaches all limitations of the claimed invention except fails to teach the display device is organic EL device.

However, it would have been obvious to obtain the display device is organic EL device in order to provide a reduction of weight and thickness device with high contrast ratio.

6. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al. (U.S. Patent No. 5,815,136) in view of Motegi et al. (U.S. Patent No. 6,025,822) and further in view of Rao (U.S. Patent No. 5,761,694).

Regarding claim 24, the combination of Ikeda and Motegi differs from claim 24 in that it does not specifically teach a D/A converter is provided between the display drive and the memory cell that converts the image signal comprising a digital signal stored in the memory cell into an analog signal, followed by supplying to the display drive. However, referring to Fig. 1A, Rao teaches a D/A converter (106) is provided between display drive (107) and memory cell (105) that converts the image signal comprising a digital signal stored in the memory cell (105) into an analog signal, followed by supplying to the display drive (107). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the D/A converter is provided between the display drive and the memory cell that converts the image signal comprising a digital signal stored in the memory cell into an analog signal, followed by supplying to the display drive as taught by Rao in the system of the combination of Ikeda and Motegi in order to provide a correspond an analog signal to display image successfully.

7. Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Jennifer T. Nguyen** whose telephone number is **703-305-3225**. The examiner can normally be reached on Mon-Fri from 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reach at **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, DC. 20231

Or faxed to: 703-872-9306 (for Technology Center 2600 only)

Art Unit: 2674

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive,
Arlington, VA, sixth-floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding
should be directed to the Technology Center 2600 Customer Service Office whose telephone
number is 703-306-0377.

JNguyen
03/25/2004


REGINA LIANG
PRIMARY EXAMINER